Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_



**UNIVERSITY**

(Karunya Institute of Technology & Sciences)

(Declared as Deemed-to-be University under Sec.3 of the UGC Act, 1956)

**End Semester Examination – Nov/Dec – 2016**

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|  |  | **Semester :** | **2016-17 ODD** |
| **Code :** | **14EC3073** | **Duration :** | **3hrs** |
| **Sub. Name :** | **FPGA FOR INDUSTRIAL APPLICATIONS** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | It is required to maintain the temperature of room at 25oC. Suggest a suitable controller with FPGA coding in VHDL language. | CO2 | 10 |
| b. | Design Excess 3 code convertor using Programmable Logic Array. | CO1 | 10 |
| (OR) | | | | |
| 2. | a. | Give the design flow process diagram of ASIC and explain the functions of each block. | CO3 | 12 |
| b. | Mention the pros and cons of SRAM technology used in Xilinx. | CO3 | 8 |
| 3. | a. | Give the importance of programmable switch matrix in Xilinx FPGA. | CO3 | 5 |
|  | b. | Implement the following function using Xilinx XC 3000. How many CLBs and LUTs are required?  F(a,b,c,d,e)=a.b.+a.b’.c+ae’+d.e | CO3 | 15 |
| (OR) | | | | |
| 4. | a. | Describe the input-output block available in Xilinx XC 4000. | CO3 | 10 |
|  | b. | Design a combinational circuit which has one data input and and manyoutput lines. Write a VHDL code for the above combinational circuit. | CO2 | 10 |
| 5. | a. | Design a Controllers for pressure Process station with Xilinx FPGA. | CO3 | 15 |
|  | b. | Justify how full- custom design have more manufacturing lead time than semicustom design. | CO3 | 5 |
| (OR) | | | | |
| 6. | a. | Explain Altera MAX 7000 Combinational Logic blocks. | CO3 | 15 |
|  | b. | Discuss importance of if else statement in behavioural style of modelling. | CO2 | 5 |
| 7. | a. | With neat sketch, explain Xilinx 3000 Configuration Logic Block. | CO3 | 15 |
|  | b. | Distinguish between: sequential and concurrent statement in VHDL. | CO2 | 5 |
| (OR) | | | | |
| 8. | a. | Mention the benefits of using semicustom design in ASIC. Explain the types of semicustom design. | CO3 | 10 |
|  | b. | Discuss the different data operators of VHDL.. | CO2 | 10 |
|  | | **Compulsory:** |  |  |
| 9. | a. | Design a PROM device to realize combinational logic using two functions  F1(x,y,z) = x’y+yz’  F2(x,y,z) = xyz+xy+xz | CO1 | 10 |
|  | b. | Design 2 bit magnitude comparator using PROM. | CO1 | 10 |

ALL THE BEST